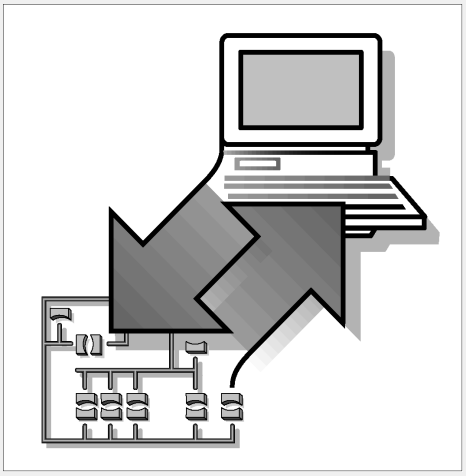
Allen-Bradley

SLC 500™ Family of Programmable Controllers

Addressing Reference Manual



Important User Information

Because of the variety of uses for the products described in this publication, those responsible for the application and use of this control equipment must satisfy themselves that all necessary steps have been taken to assure that each application and use meets all performance and safety requirements, including any applicable laws, regulations, codes and standards.

The illustrations, charts, sample programs and layout examples shown in this guide are intended solely for purposes of example. Since there are many variables and requirements associated with any particular installation, Allen-Bradley does not not assume responsibility or liability (to include intellectual property liability) for actual use based upon the examples shown in this publication.

Allen-Bradley publication SGI–1.1, Safety Guidelines for the Application, Installation, and Maintenance of Solid-State Control (available from your local Allen-Bradley office), describes some important differences between solid-state equipment and electromechanical devices that should be taken into consideration when applying products such as those described in this publication.

Throughout this manual we use notes to make you aware of safety considerations.

ATTENTION: Identifies information about practices or circumstances that can lead to personal injury or death, property damage or economic loss.

Attention statements help you to:

- identify a hazard
- avoid the hazard
- recognize the consequences

Important: Identifies information that is critical for successful application and understanding of the product.

Data Table Addressing for the SLC 500™ Family of Processors

Introduction

This addressing reference helps you specify data table addresses in SLC 500™ fixed and modular programmable controllers. It contains information for the following processors:

- all SLC 500 Fixed Programmable Controllers
- The following SLC 500 Modular Programmable Controllers
  - SLC 5/01 CPU
  - SLC 5/02 CPU
  - SLC 5/03 CPU

Locating Addressing Information

For specific information about the content of data table files, consult the:

- PLC® programmer, who assigns data to specific memory locations
- SLC 500 Fixed Hardware Style Installation and Operation Manual, publication 1747–NI001.
- SLC 500 Modular Hardware Style Installation and Operation Manual, publication 1747–NI002.
- Advanced Programming Software (APS) User's Manual, publication 1747–NM002.

Important: Throughout this publication we use **$** as the logical address identifier. This is an entry for INTERCHANGE software. It is also an entry for 6200 programming software in sending a message from other stations to a SLC 500 processing station. It is not used in 6200 programming software for internal addressing.

Memory Map

Table A shows the logical arrangement of the data table for SLC 500 processors.

Table A
Data Table Memory Map

File Number	File Type	Logical Address	Comments
0	OUTPUT IMAGE	$O:0 to $O:30	
1	INPUT IMAGE	$I:0 to $I:30	
2	STATUS	$S:0 to $S:n	**See Note 1**
3	BINARY	$B3:0 to $B3:255	
4	TIMER	$T4:0 to $T4:255	
5	COUNTER	$C5:0 to $C5:255	
6	CONTROL	$R6:0 to $R6:255	
7	INTEGER	$N7:0 to $N7:255	
8	FLOATING–POINT	$F8:0 to $F8:255	**See Note 2**
9	NETWORK	$x9:0 to $x9:255	**See Note 3**
10 thru 255	USER DEFINED	$x10:0 to $x255:255	**See Note 4**

Notes

1 Address range is processor specific; see Logical Addressing for the Status Elements section.

2 Only the SLC 5/03 series B processor supports floating-point data type. Do not use this area for processors that do not support floating-point data.

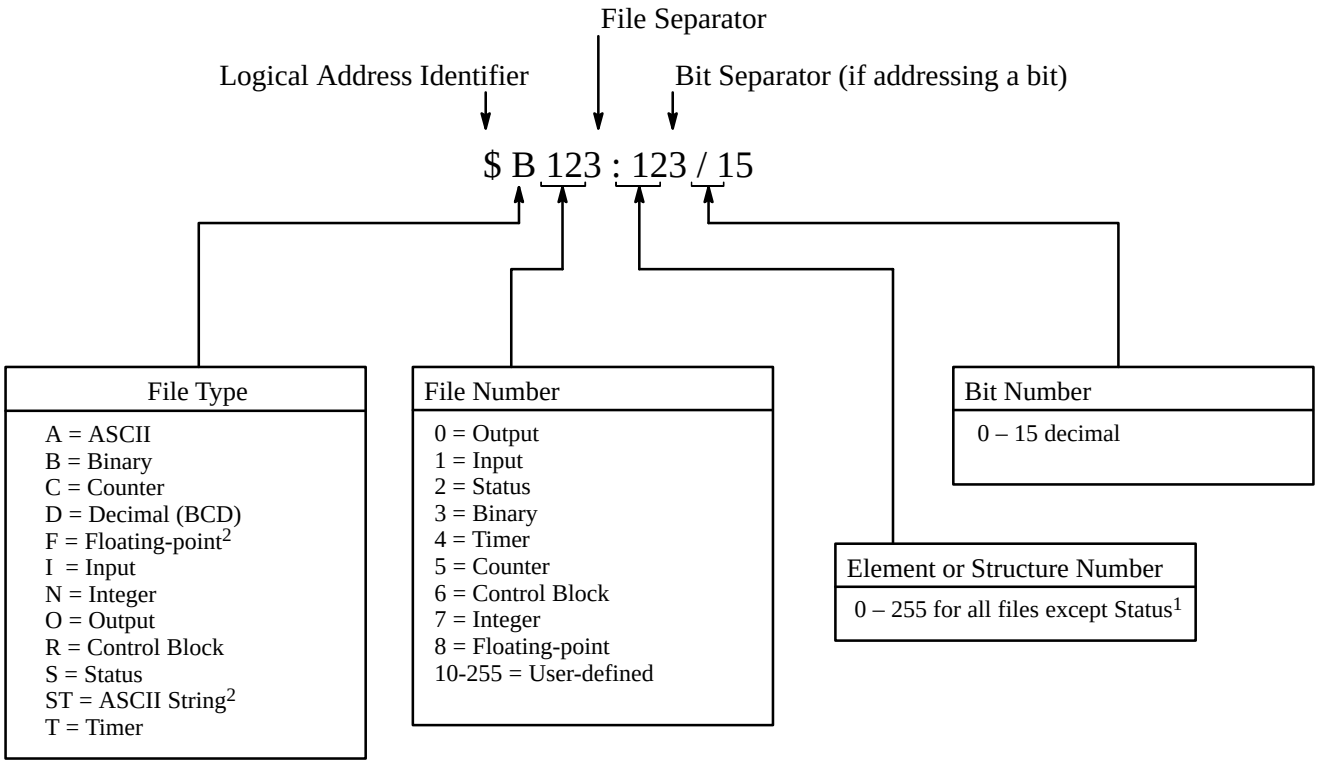
3 If non SLC 500 devices exist on the DH-485 link, use this area for network transfer. You can use either binary (B) or integer (N) file types by specifying the appropriate letter for *x*. Otherwise, you can use file 9 for user-defined files.

4 Use this area when you need more binary, timer, counter, control, integer, floating-point, or network files that will fit in the reserved files. You can use binary (B), timer (T), counter (C), control (R), integer (N), floating-point (F), or transfers (B and/or N) file types by specifying the appropriate letter for *x*. You cannot use this area for output image, input image, and/or status files.

General Format for Logical ASCII Addressing

Figure 1 illustrates the general format for logical addressing in the data table.

Figure 1
General Format for Logical Addressing



Notes:
[1] The number of elements (words) in the status file is processor dependent; see Logical Addressing for the Status Element section.
[2] ASCII string, floating-point, and network file types are not available on SLC 500, SLC 5/01, SLC 5/02, SLC 5/03 processors.

You can address individual bits for the following elements in a data table file by absolute bit number (0 thru 4095):

- binary
- control block
- input image
- integer
- output image
- status

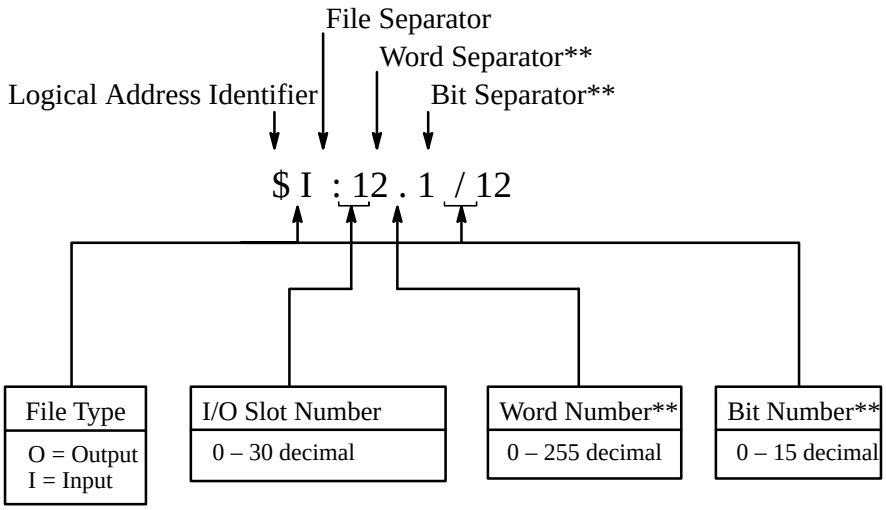
Logical Addressing for the Input/Output Image Elements

The file for output image elements is file 0 of the data table. This file accommodates up to 256 output image elements.

The file for input image elements is file 1 of the data table. This file accommodates up to 256 input image elements.

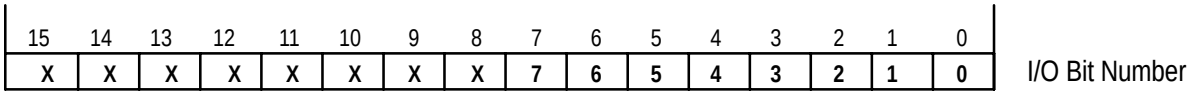
Each I/O image element consists of one 16-bit word. You can address an I/O image element in its entirety of you can address any particular input or output bit of an element individually.

Figure 2
Logical Addressing for I/O Image Elements



* Required only when addressing to the bit level.
** Required only when addressing 24- and 32-bit I/O.

Figure 3
Bit Map of I/O Image Element for 8-bit Discrete I/O



X = Not Used

Figure 4
Bit Map of I/O Image Element for 16-bit Discrete I/O

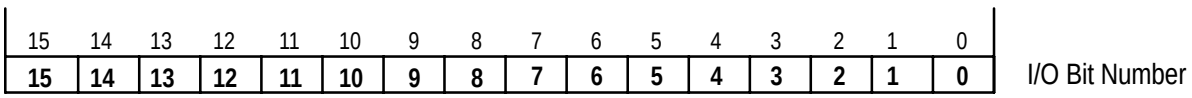


Figure 5
Bit Map of I/O Image Element for 24-bit Discrete I/O

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Word 0	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	I/O Bit Number
Word 1	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**	I/O Bit Number

Figure 6
Bit Map of I/O Image Element for 32-bit Discrete I/O

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Word 0	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	I/O Bit Number
Word 1	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	I/O Bit Number

Table B
Parameters of I/O Elements

Description	PLC Data Type	Valid Range
Input Element	signed word	–32,768 thru +32,767
Output Element	signed word	–32,768 thru +32,767

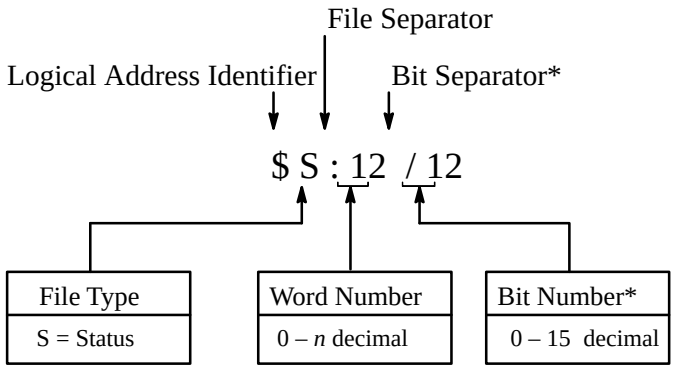
Table C
Examples for I/O Element 3 in Slot 5

To address the	Use this form
Entire Input Element	$I:5.3
Input Bit 6	$I:5.3/6
Entire Output Element	$O:5.3
Output Bit 6	$O:5.3/6

Logical Addressing for the Status Elements

The file for status elements is file 2 of the data table. The number of status elements in this file (*n*) is processor dependent, see Figure 8.

Figure 7
Logical Addressing for Status Elements



*Required only when addressing to the bit level..

For specific information about status elements, refer to the Advanced Programming Software (APS) User's Manual, publication 1747-NM002.

Table D
Parameters of Status Words

Description	PLC Data Type	Valid Range
Status Element	signed word	–32,768 thru +32,767

Table E
Examples for Status Element 3 in the Default File (File 2)

To address the	Use this form
Entire Element	$S:3 or $S2:3
Tenth Data Bit	$S:3/9 or $S2:3/9

Figure 8
Status file Memory Map for SLC Processors[1]

Word	Description		Word	Description
0	Arithmetic and Scan Stat Flags		42	Time-of-Day Seconds
1	Processor Mode, Status, and Control		43	Reserved
2	Processor Alternate Mode, Status, and Control		44	Reserved
3	Current and Watchdog Scan Timers		45	Reserved
4	Timebase		46	DII File Number
5	Minor Error Bits		47	DII Input Slot
6	Major Error Bits		48	DII Mask
7	Suspend Code		49	DII Compare Value
8	Suspend File		50	DII Down Count
9	Network – Active Node Table word 0		51	DII Return Mask
10	Network – Active Node Table word 1		52	DII Accumulator
11	I/O Slot Enable/Disable Flags word 0		53	Reserved
12	I/O Slot Enable/Disable Flags word 1		54	Reserved
13	Math Register word 0		55	Last DII ISR Scan Time
14	Math Register word 1		56	Maximum DII ISR Scan Time
15	Node Address and Baud Rate		57	Processor Operating System Catalog Number
16	Test Single Step – Start at Rung Number		58	Processor Operating System System Series
17	Test Single Step – Start at File Number		59	Processor Operating System Release Number
18	Test Single Step – Stop Before Rung Number		60	Hardware Catalog Number
19	Test Single Step – Stop Before File Number		61	Hardware Series
20	Test Report – Fault/Powerdown Rung Number		62	Hardware Revision
21	Test Report – Fault/Powerdown File Number		63	User Program Type
22	Maximum Observed Scan Time		64	User Program Functional Index
23	Average Scan Time		65	User RAM Size
24	Index Register		66	Flash EEPROM Size
25	I/O Interrupt Pending word 0		67	Channel 0 Active Node Table word 0
26	I/O Interrupt Pending word 1		68	Channel 0 Active Node Table word 1
27	I/O Interrupt Enabled word 0		69	Channel 0 Active Node Table word 2
28	I/O Interrupt Enabled word 1		70	Channel 0 Active Node Table word 3
29	User Fault Routine File Number		71	Channel 0 Active Node Table word 4
30	STI (selectable timed interrupt) Time Interval		72	Channel 0 Active Node Table word 5
31	STI (selectable timed interrupt) File Number		73	Channel 0 Active Node Table word 6
32	I/O Interrupt Executing		74	Channel 0 Active Node Table word 7
33	Extended Processor Mode, Status, and Control		75	Channel 0 Active Node Table word 8
34	Reserved		76	Channel 0 Active Node Table word 9
35	Current Scan Time 1 msec		77	Channel 0 Active Node Table word 10
36	Extended Minor Error Bits		78	Channel 0 Active Node Table word 11
37	Calendar Year		79	Channel 0 Active Node Table word 12
38	Calendar Month		80	Channel 0 Active Node Table word 13
39	Calendar Day		81	Channel 0 Active Node Table word 14
40	Time-of-Day Hours		82	Channel 0 Active Node Table word 15
41	Time-of-Day Minutes			

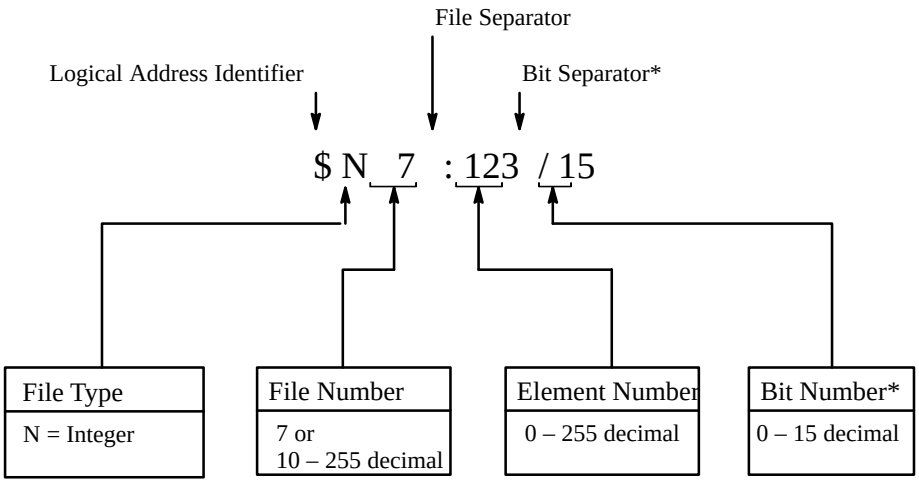
1 Not all processors support all status words. SLC 500 and SLC 5/01 processors only support words 0 – 15. SLC 5/02 processors only support words 0 – 32. SLC 5/03 processors support words 0 – 82

Logical Addressing for Integer Elements

The recommended default file for integer elements is file 7 of the data table. This file accommodates up to 256 integer elements. If your application requires more than 256 integer elements, specify one or more files (10 – 255) in the user-defined area of the data table in addition to file 7.

Each integer element consists of one 16-bit word. You can address an integer element in its entirety or you can address any particular data bit of an element individually.

Figure 9
Logical Addressing for Integer Elements



*Required only if addressing to the bit level.

Figure 10
Bit Map of the Integer Element

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DB15	**DB14**	**DB13**	**DB12**	**DB11**	**DB10**	**DB9**	**DB8**	**DB7**	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**

DB = Data Bit

Table F
Parameters of Integer Elements

Description	PLC Data Type	Valid Range
Integer Element	signed word	–32,768 thru +32,767
DB *n*	—	0 or 1

Table G
Examples for Integer Element 3 in the Default File (File 7)

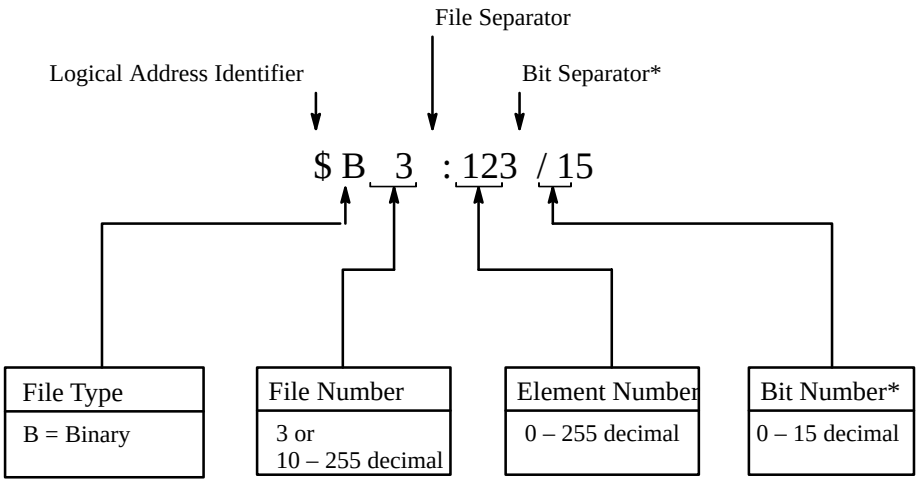
To address the	Use this form
Entire Element	$N7:3
Tenth Data Bit	$N7:3/9

Logical Addressing for Binary Elements

The recommended default file for binary elements is file 3 of the data table. This file accommodates up to 256 binary elements. If your application requires more than 256 binary elements, specify one or more files (10 – 255) in the user-defined area of the data table in addition to file 3.

Each binary element consists of one word. You can address a binary element in its entirety or you can address any particular data bit of an element individually.

Figure 11
Logical Addressing for Binary Elements



*Required only if addressing to the bit level.

Figure 12
Bit Map of the Binary Element

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DB15	**DB14**	**DB13**	**DB12**	**DB11**	**DB10**	**DB9**	**DB8**	**DB7**	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**

DB = Data Bit

Table H
Parameters of Binary Elements

Description	PLC Data Type	Valid Range
Binary Element	signed word	–32,768 thru +32,767
DB *n*	—	0 or 1

Table I
Examples for Binary Element 2 in the Default File (File 3)

To address the	Use this form
Entire Element	$B3:2
Tenth Data Bit	$B3:2/9

Logical Addressing for Floating-Point Elements

The recommended default file for floating-point elements is file 8 of the data table. This file accommodates up to 256 floating-point elements. If your application requires more than 256 floating-point elements, specify one or more files (10 – 255) in the user-defined area of the data table in addition to file 8.

Each floating-point element consists of two words. You must address the floating-point element in its entirety.

Figure 13
Logical Addressing for Floating-Point Elements

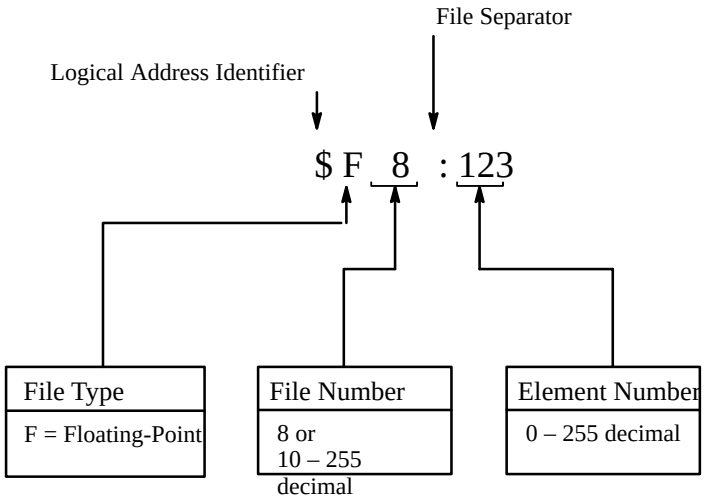


Figure 14
Bit Map of the Floating-Point Element

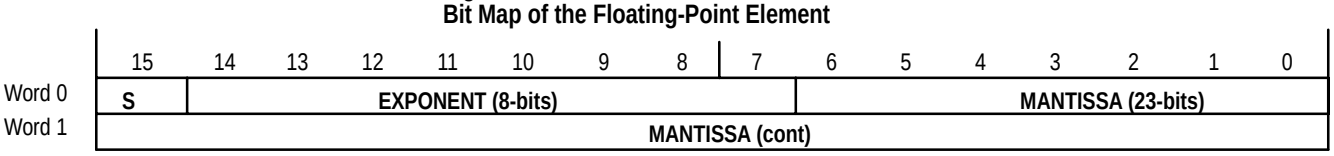


Table J
Parameters of Floating-Point Elements

Description	PLC Data Type	Valid Range
Floating-Point Element	IEEE Float	± 1.1754944 E–38 thru ± 028237 E+38

Table K
Examples for Floating-Point Element 9 in the Default File (File 8)

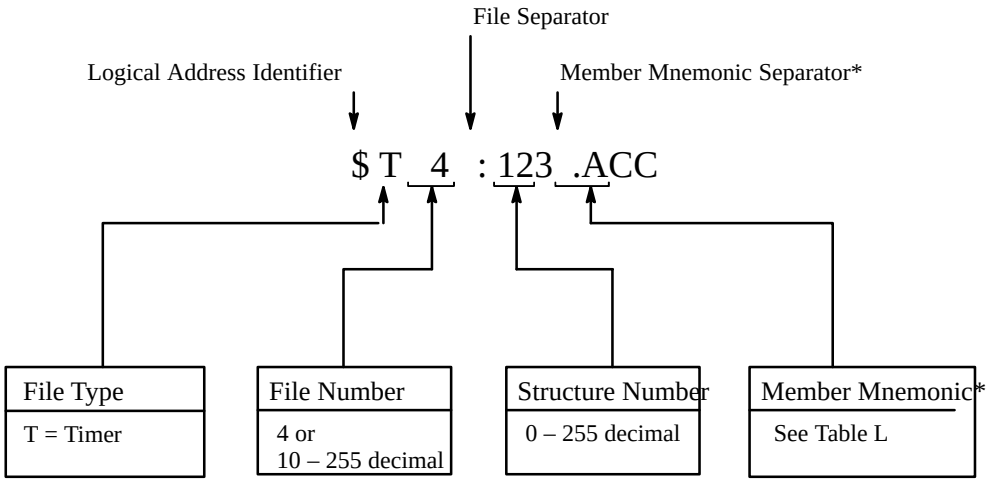
To address the	Use this form
Entire Element	$F8:9

Logical Addressing for Timer Structures

The recommended default file for timer structures is file 4 of the data table. This file accommodates up to 256 timer structures. If your application requires more than 256 timer structures, specify one or more files (10 – 255) in the user-defined area of the data table in addition to file 4.

Each timer structure consists of three words. You can address a timer structure in its entirety or you can address any particular member of a structure individually.

Figure 15
Logical Addressing for Timer Structures



*Required only if addressing to the member level.

Figure 16
Bit Map of the Timer Structure

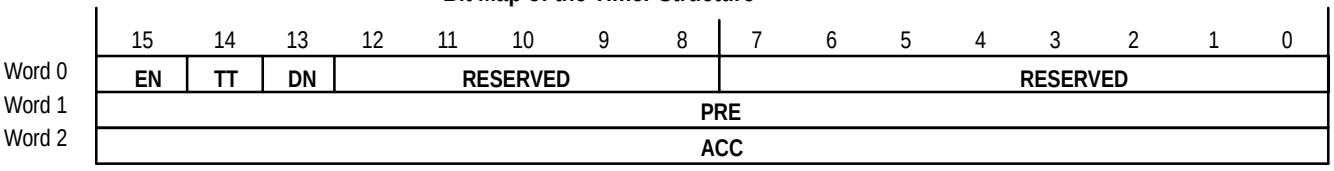


Table L
Mnemonics used with Timers

Mnemonic	Description	PLC Data Type	Valid Range
EN	Enabled	bit	0 or 1
TT	Timer Timing	bit	0 or 1
DN	Done	bit	0 or 1
PRE[1]	Preset Value	signed word	0 thru +32,767
ACC[1]	Accumulated Value	signed word	0 thru +32,767

[1]The lower limit of valid range for PRE and ACC is zero not –32,768 even though the PLC data type is signed word.

Table M
Examples for Timer Structure 3 in the Default File (File 4)

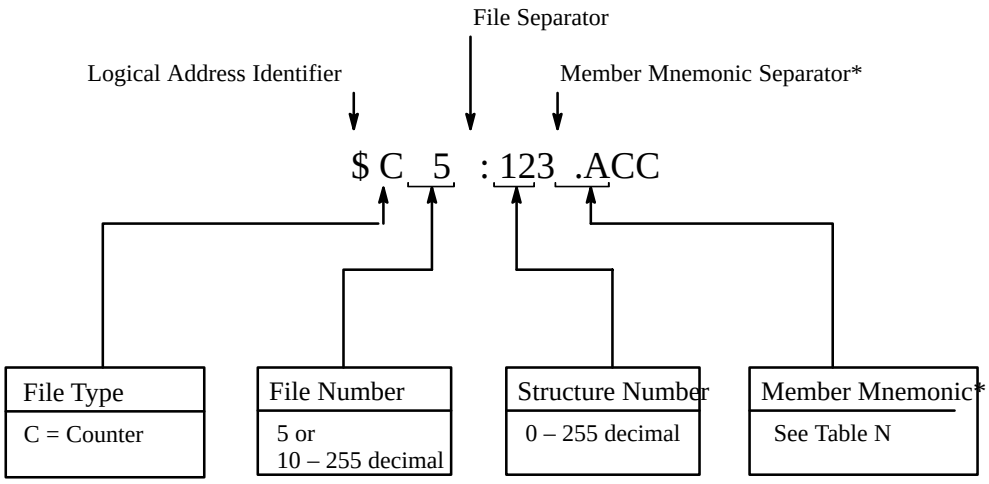
To address the	Use this form
Entire Structure	$T4:3
Enabled Bit	$T4:3.EN or $T4:3/EN
Timing Bit	$T4:3.TT or $T4:3/TT
Done Bit	$T4:3.DN or $T4:3/DN
Preset Value	$T4:3.PRE
Accumulated Value	$T4:3.ACC

Logical Addressing for Counter Structures

The recommended default file for counter structures is file 5 of the data table. This file accommodates up to 256 counter structures. If your application requires more than 256 counter structures, specify one or more files (10 – 255) in the user-defined area of the data table in addition to file 5.

Each counter structure consists of three words. You can address a counter structure in its entirety or you can address any particular member of a structure individually.

Figure 17
Logical Addressing for Counter Structures



*Required only if addressing to the member level.

Figure 18
Bit Map of the Counter Structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word 0	CU	CD	DN	OV	UN	UA[1]	RESERVED		RESERVED							
Word 1	PRE															
Word 2	ACC															

Table N
Mnemonics used with Counters

Mnemonic	Description	PLC Data Type	Valid Range
CU	Count Up Enabled	bit	0 or 1
CD	Count Down Enabled	bit	0 or 1
DN	Done	bit	0 or 1
OV	Overflow	bit	0 or 1
UN	Underflow	bit	0 or 1
UA[1]	Update Accumulator	bit	0 or 1
PRE	Preset Value	signed word	–32,768 thru +32,767
ACC	Accumulated Value	signed word	–32,768 thru +32,767

[1]This bit available only in SLC 500 fixed-style processors equipped with an HSC (high-speed counter). In addition, the lower limit of valid range for PRE and ACC is zero, not –32,768 for these processors.

Table O
Examples for Counter Structure 7 in the Default File (File 5)

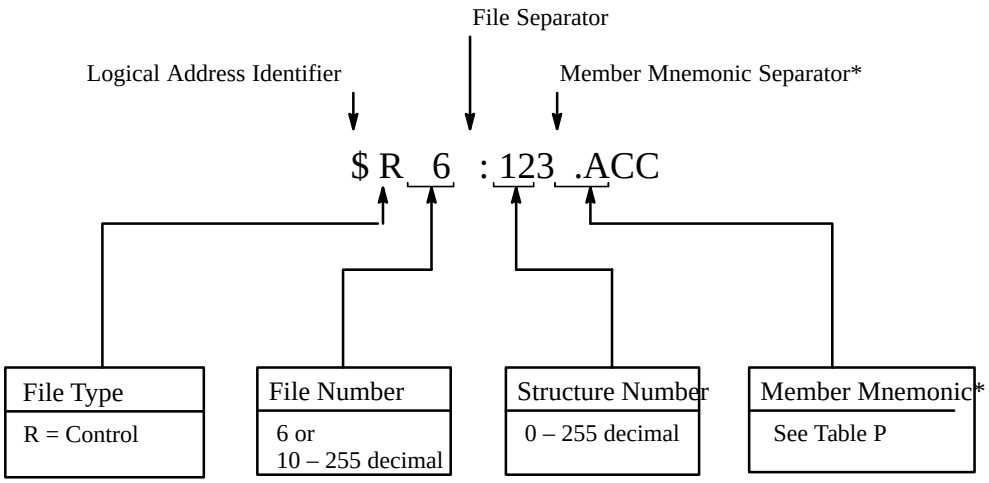
To address the	Use this form
Entire Structure	$C5:7
Count Up Enabled Bit	$C5:7.CU or $C5:7/CU
Count Down Enabled Bit	$C5:7.CD or $C5:7/CD
Done Bit	$C5:7.DN or $C5:7/DN
Overflow Bit	$C5:7.OV or $C5:7/OV
Underflow Bit	$C5:7.UN or $C5:7/UN
Update Accumulator Bit	$C5:7.UA or $C5:7/UA
Preset Value	$C5:7.PRE
Accumulated Value	$C5:7.ACC

Logical Addressing for Control Block Structures

The recommended default file for control block structures is file 6 of the data table. This file accommodates up to 256 control block structures. If your application requires more than 256 control block structures, specify one or more files (10 – 255) in the user-defined area of the data table in addition to file 6.

Each control block structure consists of three words. You can address a control block structure in its entirety or you can address any particular member of a structure individually.

Figure 19
Logical Addressing for Control Block Structures



*Required only if addressing to the member level.

Figure 20
Bit Map of the Control Block Structure

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word 0	EN	EU	DN	EM	ER	UL	IN	FD	RESERVED							
Word 1	LEN															
Word 2	POS															

Table P
Mnemonics used with Control Blocks

Mnemonic	Description	PLC Data Type	Valid Range
EN	Enabled	bit	0 or 1
EU	Unloading Enabled	bit	0 or 1
DN	Done	bit	0 or 1
EM	Stack Empty	bit	0 or 1
ER	Error	bit	0 or 1
UL	Unload (shift bit only)	bit	0 or 1
IN	Inhibit Comparisons	bit	0 or 1
FD	Found (SQC only)	bit	0 or 1
LEN	Length	signed word	–32,768 thru +32,767
POS	Position	signed word	–32,768 thru +32,767

Table Q
Examples for Control Block Structure 0 in the Default File (File 6)

To address the	Use this form
Entire Structure	$R6:0
Enabled Bit	$R6:0.EN or $R6:0/EN
Unloading Enabled Bit	$R6:0.EU or $R6:0/EU
Done Bit	$R6:0.DN or $R6:0/DN
Stack Empty Bit	$R6:0.EM or $R6:0/EM
Error Bit	$R6:0.ER or $R6:0/ER
Unload Bit	$R6:0.UL or $R6:0/UL
Inhibit Comparisons Bit	$R6:0.IN or $R6:0/IN
Found Bit	$R6:0.FD or $R6:0/FD
Length	$R6:0.LEN
Position	$R6:0.POS

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Customer Support

If you need additional assistance on using your software, Allen-Bradley offers telephone and on-site product support.

For technical assistance on the telephone, first contact your local sales office, distributor, or system integrator. If additional assistance is needed, then contact your local Customer Support Center.

For assistance that requires on-site support, contact your local sales office, distributor, or system integrator. During non-office hours, contact the Allen-Bradley 24-hour Hot Line at 1-800-422-4913 in the United States or contact your local Customer Support Center outside the United States.

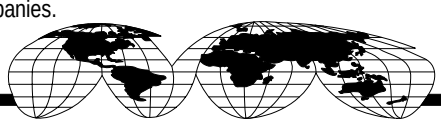
Customer Support Center phone numbers:

Region or Area	Customer Support Center Telephone Number
Canada (Cambridge, Ontario)	519-623-1810
Latin America (Mexico)	52-5-259-0400
United Kingdom (Milton Keynes)	44-908-838800
France (Paris)	(33-1) 3067-7200
Germany (Gruiten)	(49) 2104-6900
Italy (Milan)	(39-2) 939-721
Asia Pacific (Hong Kong)	(852) 887-4788
Spain (Barcelona)	(34-3) 331-7004

Rockwell Automation

Allen-Bradley

Allen-Bradley, a Rockwell Automation Business, has been helping its customers improve productivity and quality for 90 years. We design, manufacture, and support a broad range of control and automation products worldwide. They include logic processors, power and motion control devices, man-machine interfaces, sensors, and a variety of software. Rockwell is one of the world's leading technology companies.



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